UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,009	09/22/2003	Joo S. Choi	2008.007800/03-0623	1907

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EXAMINER
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ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 March 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-3 and 5-29</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-3,6,7,10-14,16-26,28 and 29</u> is/are rejected.

7)☒ Claim(s) <u>8,9,15 and 27</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Detailed Action

1.   Claims 1-3 and 5-29 are presented for examination. This office action is in

response to the amendment filed on 3/6/2006.

2.   Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Objections

3.   Claims 1-3 and 5-29 are objected to because of the following informalities:

As to claims 1-3 and 5-29, it appears that added limitations (i.e. determining the

desired burst length information or latency information based on the nature of the

received memory request and access the memory using different burst lengths without

requiring re programming of a register) were not described in the specification at the

time the application was filed.

As to claim 6, in line 1, "4" should be changed to –1—for clarity.

Appropriate correction/explanation is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed
publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4.   Claim 29 is rejected under 35 U.S.C. 102(a) as being anticipated by Fanning US Patent No. 6,615,308.

As to claim 28, Fanning discloses the invention as claimed. Fanning discloses an apparatus, comprising: a controller (Fig. 5 ref 500) adapted to receive requests to access memory (Fig. 5 read and write request) and access the memory using different burst length without requiring reprogramming of a register holding information relating to burst length (col. 3 lines 20-35)

5.   Claims 1-2, and 5-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli US Patent No. 6,675,270.

As to claims 1 and 22, Arimilli discloses the invention as claimed. Arimilli discloses a method, comprises receiving a command (Fig. 5 RAS, CAS and data) from a controller (Fig. 2 Ref. 235) to access a memory (Fig. 2 Ref. 234) in response to a memory request from a source (Fig. 2 Ref. 110); determining the desired burst length (Fig. 3 Ref. 303 and col. 2 lines 63+ & col. 4 lines 33-35) information based on the nature of received memory request; and providing data (Fig. 5 Ref. Data) to or from the memory in response to the command based on at least one of the burst length information and the latency information.

As to claim 2, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein receiving a command comprises receiving at least one of a

READ operation and WRITE operation to access the contents of the memory (Fig. 5,

Read and Write).

As to claim 5, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein determining the desired burst length information comprises

determining the desired burst length information based on an amount of data to be

retrieved from the memory (col. 2 lines 58-60 and 63+).

As to claim 6, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein determining the burst length information comprises

determining the burst length information based on the source that provided the memory

request (Fig. 3 Ref 303).

As to claim 7, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein providing the data comprises providing the data comprises

providing the data in response to receiving the burst length information or latency

information over a redundant address line to the memory (col. 2 lines 63+ and Fig. 3

Ref 303).

As to claim 10, Arimilli discloses the invention as claimed. Arimilli discloses an apparatus, comprises a controller (Fig. 2 Ref. 235) adapted to: provide a command (Fig. 5 CAS, RAS and Data) to access a memory array (Fig. 2 Ref. 234) in response to a memory request from a source (Fig. 2 Ref. 110); determining at least one of burst length information and latency information based on the nature of the memory request received from the source (Fig. 3 Ref 303 and col. 2 lines 63+) and receive data (Fig. 5 Data) from the memory array based on at least one of the burst length information and the latency information.

As to claim 11, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to issue a READ operation access the contents of the memory (Fig. 5 Read and write).

As to claim 12, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to provide at least one of the burst length information and the latency information contemporaneously with the command to access the memory (col. 2 lines 63+).

As to claim 13, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a request from a

main client, wherein the first preselected value is less than the second preselected

value (and col. 2 lines 63+).

As to claim 14, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein the controller is adapted to provide at least one of the burst

length information and latency information over a redundant address line to the

memory (Fig. 3 Ref. 303).

As to claim 16, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein the controller is adapted to issue a WRITE command and

adapted to provide write latency information contemporaneously with the WRITE

command (and col. 2 lines 63+).

As to claim 17, Arimilli discloses the invention as claimed. Arimilli discloses a

system, comprises a memory array (Fig. 3 Ref. 234), and a controller (Fig. 3 ref. 235)

communicatively coupled to the memory array, the controller adapted to: provide a

command (Fig. 5 RAS, CAS, and Data) to access the memory array in response to a

memory request (Fig. 3) form a source (Fig. 1 Ref. 110); and determine at least one of

burst length information and latency information (Fig. 3 Ref. 303 and col. 2 lines 63+)

based on the nature of the received memory request; and wherein the memory array is

adapted to provide or receive data (Fig. 5 Data) based on at least one of the burst

length information and the latency information.

As to claim 18, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to issue at least one of a READ operation and WRITE operation access the contents of the memory (Fig. 5 read and write).

As to claim 19, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to provide at least one of the burst length information and the latency information contemporaneously with the command to access the memory (col. 2 lines 63+).

As to claim 20, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to provide a burst length of a first preselected value in response to receiving a request from a peripheral client and a burst length of a second preselected value in response to receiving a request from a main client, wherein the first preselected value is less than the second preselected value (Col. 2 lines 63+).

As to claim 21, Arimilli discloses the invention as claimed the above. Arimilli further discloses wherein the controller is adapted to provide at least one of the burst length information and latency information over a redundant address line to the memory (col. 2 lines 63+).

As to claim 23, Arimilli discloses the invention as claimed. Arimilli discloses an

apparatus, comprises a memory (Fig. 2 ref. 234) adapted to: receive a request (Fig. 5)

to access contents of the memory; receive, from the memory controller, at least one of

burst length information (Fig. 3 ref. 303 and col. 2 lines 63+) and latency information

based on the nature of the memory request ; and provide data (Fig. 5 Data) from the

memory based on at least one of the burst length information and the latency

information.

As to claim 24, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein memory is adapted to receive at least one of the burst length

information and the latency information contemporaneously with the command to

access the memory (col. 2 lines 63 thru col. 3 line 2).

As to claim 25, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein the memory is adapted to receive a burst length of a first

preselected value in response to the controller receiving a request from a peripheral

client and a burst length of a second preselected value in response to the controller

receiving a request from a main client, wherein the first preselected value is less than

the second preselected value (col. 2 lines 63 thru col. 3 line 2).

As to claim 26, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein the memory is adapted to receive at least one of the burst

length information and latency information over a redundant address line (col. 2 lines

63 thru col. 3 line 2).

As to claim 28, Arimilli discloses the invention as claimed the above. Arimilli

further discloses wherein the memory is adapted to receive a WRITE command and

adapted to receive write latency information contemporaneously with the WRITE

command (col. 2 lines 63 thru col. 3 line 2 and Fig. 5 Read and Write).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be
> patented and the prior art are such that the subject matter as a whole would have been obvious
> at the time the invention was made to a person having ordinary skill in the art to which said
> subject matter pertains. Patentability shall not be negatived by the manner in which the invention
> was made.

6.   Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli

US Patent No. 6,675,270 in view of Hampel et al. (Hampel) U.S. Patent No. 6,542,416.

As to claim 3, Arimilli discloses the invention as claimed above. Arimilli further

discloses command includes the burst length with the addresses and other standard

parameter (col. 4 lines 33-35), however, Arimilli does not specifically disclose wherein

receiving the latency information comprises receiving at least one of column address

strobe latency information and write latency information.

Hampel discloses wherein receiving the latency information comprises receiving

at least one of column address strobe latency information and write latency information

(col. 2 lines 55-59) for the purpose of providing a capability of better supporting the

applied work load (col. 2 lines 55-59) thereby result in better performances and

increased bandwidth.

Accordingly, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to incorporate wherein receiving the latency

information comprises receiving at least one of column address strobe latency

information and write latency information as taught by Hampel in the system of Arimilli

for the advantages stated above.

Allowable Subject Matter

7.   Claims 8, 9, 15, 27 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

Conclusion

1.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.   See attached PTO-892.

2.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

3.   When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections.   See 37 C.F.R. ' 1.111(c).

4.   When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Hong Kim whose telephone number is (571) 272-4181.

The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general

nature or relating to the status of this application should be directed to the TC 2100

whose telephone number is (571) 272-2100.

6.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

7.   **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service
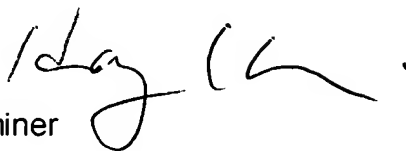Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
April 5, 2006